## REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-21 in the application. In the present response, the Applicants have amended Claims 1, 8, and 15. Support for the amendment can be found, for example, in paragraph 60 of the original specification. This amendment has been made solely to address the §112, second paragraph rejection of the pending Final Rejection and not to add any new matter. Therefore, since no new matter has been presented, a new search is not needed. No other claims have been canceled or added in the present response. Accordingly, Claims 1-21 are currently pending in the application.

### I. Rejection of Claims 1-21 under 35 U.S.C. §112

The Examiner has rejected Claims 1-21 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention. More specifically, the Examiner has stated that the phrase regarding the rate in independent Claims 1, 8, and 15 could be interpreted to modify the sequencing of the thread or to modify the exiting of the thread. In response, the Applicants have amended independent Claims 1, 8, and 15 to clearly and distinctly claim that the rate modifies the sequencing of the thread through the entire miss fulfillment FIFO. As such, the context controller subsystem is configured to sequence the thread through a miss fulfillment FIFO at a rate equal to the pipeline latency of the multi-thread execution pipeline loop, where pipeline latency is defined as the rate at which data or a thread traverses a multi-thread execution pipeline loop. (*See* paragraphs 47 and 60.) Accordingly, the Applicants respectfully request the Examiner to withdraw the §112, second paragraph rejection of Claims 1-21 and allow issuance thereof.

## II. Rejection of Claims 1-14 under 35 U.S.C. §103

The Examiner has rejected Claims 1-14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,933,627 to Parady in view of an article by Li, et al., entitled "The Effects of STEF in a Finely Parallel Multithreaded Processors," ©1995 IEEE. The Applicants respectfully disagree. More specifically, the Applicants disagree since the combination of Parady and Li does not teach or suggest a thread sequencing through an entire miss fulfillment FIFO at a rate having a period associated with a pipeline latency before exiting therefrom as recited in independent Claims 1 and 8.

The Examiner notes that Parady does not explicitly teach a miss fulfillment FIFO buffer **and** storing a thread in the miss fulfillment FIFO to prevent the thread from executing until a device request if fulfilled, the thread sequencing through the entire miss fulfillment FIFO before exiting therefrom at a period associated with a pipeline latency. The Examiner cites Li to cure these deficiencies of Parady. (*See* Examiner's Final Rejection mailed January 26, 2007, pages 4-5.)

Li teaches a Finely Parallel Multithreaded Processor (FPMP) architecture with a separate instruction cache for each thread slot and an Instruction Scheduling Unit (ISU) having a FIFO register for each thread slot that schedules instructions and issues them to the appropriate functional unit. The ISU examines the available thread in a FIFO register to see if it is ready. If the FIFO register of a thread slot does not have an instruction that is ready, the particular thread slot FIFO will hold the instruction and the ISU will move on, based on a round robin scheduling strategy, to examine a next thread slot FIFO register to see if it has a ready instruction. If the ISU finds the instruction of a thread slot FIFO register it is examining is ready, it will then issue that

instruction to the appropriate functional unit on the next clock cycle. Once a held un-issued instruction in a particular thread slot FIFO register becomes ready, it will be issued to the appropriate functional unit on a next clock cycle after the ISU returns back to it (based on the round robin scheduling strategy) and finds that is it ready after examination. (*See* Li, pages 319-320, Section 2, paragraphs 2-6. Emphasis added.)

Thus, the amount of time the thread slot FIFO register holds an un-issued instruction depends on the amount of time it takes to make an un-issued instruction ready (*e.g.*, for the source operands to become available) plus the amount of time it takes for the ISU to return to it after finding other thread slot FIFO registers not ready. This could be several clock cycles. Therefore, even assuming *arguendo* that the clock cycle in Li is equivalent to the pipeline latency as asserted by the Examiner, (*see* Examiner's Final Rejection mailed January 26, 2007, page 5) Li does not teach or suggest an instruction will sequence through the entire thread slot FIFO register at a rate having a period associated with a pipeline latency. Instead, Li teaches an instruction will sequence through the entire FIFO at a rate based on when an instruction is ready and the next clock cycle. Li will hold an instruction until it is ready and then issue it to the appropriate execution pipeline on a next clock cycle. As such, Li does not teach or suggest a thread sequences through an **entire** miss fulfillment FIFO **at the pipeline latency** as presently claimed.

Additionally, the cited combination of Parady and Li does not teach a context switching system comprising **a** FIFO as recited in independent Claims 1 and 8. Instead, Li teaches FIFO registers **for each** thread slot are provided in the ISU. (See Li, page 320, Section 2, paragraph 6.) Thus, Li does not teach a **single** FIFO as presently claimed, but rather, a FIFO for each thread slot.

For at least the reasons stated above, the cited combination of Parady and Li does not teach or suggest all of the claim limitations of independent Claims 1 and 8. Therefore, the cited combination does not provide a *prima facie* case of obviousness for Claims 1 and 8 and Claims that depend thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 1-14 and allow issuance thereof.

Furthermore, with regard to dependent Claims 4 and 11, the cited combination of Parady and Li does not teach or suggest reinserting a thread into a multi-thread execution pipeline loop at a beginning position after the thread exits a miss fulfillment FIFO. On the contrary, Li teaches that the thread is held in the FIFO until it is ready and then the thread is issued directly to the functional unit. (*See* Li, pages 319-320, Section 2, paragraphs 3 and 6.)

## III. Rejection of Claims 15-21 under 35 U.S.C. §103

The Examiner has rejected Claims 15-21 under 35 U.S.C. §103(a) as being unpatentable over Parady in view of U.S. Patent No. 5,509,006 by Wilford, *et al.* in further view of Li. The Applicants respectfully disagree.

As argued above, the combination of Parady and Li does not provide a *prima facie* case of obviousness for independent Claims 1 and 8. This is based on the combination of Parady and Li failing to teach or suggest a thread sequencing through an entire miss fulfillment FIFO at a rate having a period associated with a pipeline latency before exiting therefrom. The Examiner has not asserted, nor do the Applicants find where, Wilford cures this deficiency of Parady and Li. On the contrary, the Examiner has stated that Parady has not taught a tree engine that parses data with PDUs and cites Wilford to teach this limitation of independent Claim 15. (*See* Examiner's Final Rejection

mailed January 26, 2007, page 11.) As such, the cited combination of Parady, Li, and Wilford does not cure the noted deficiency of Parady and Li and, therefore, does not provide a *prima facie* case of obviousness of independent Claim 15 and Claims that depend thereon. Accordingly, the Applicants respectfully request the Examiner to withdraw the §103(a) rejection of Claims 15-21 and allow issuance thereof.

## IV. Comment on Reference

The Applicants reserve further review of the references cited on but not relied upon if relied upon in the future.

## III. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 08-2395.

Respectfully submitted,

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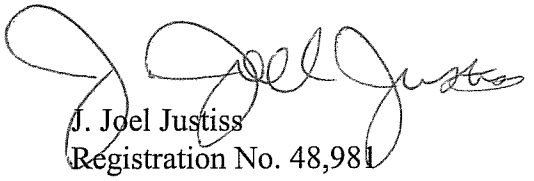

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